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A maskless laser-write lithography processing of thin-film transistors on a hemispherical surface

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ABSTRACT

We report on the design and fabrication methods for a hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) on a non-planar substrate using laser-write lithography (LWL). Level-to-level alignment with a high accuracy is demonstrated using LWL method. The fabricated a-Si:H TFT exhibits a field-effect mobility of 0.27 cm^2/V s, threshold voltage of 4.9 V and on/off current ratio of $\sim 6 \times 10^6$ in a saturation regime. The obtained results demonstrate that it is possible to fabricate the a-Si:H TFTs and complex circuitry on a curved surface, using a well-established a-Si:H TFT technology in combination with the maskless lithography, for hemispherical or non-planar sensor arrays.

1. Introduction

There is increasing demands for the implementation of electronic and optoelectronic systems on non-planar surfaces for their diverse and unique applications: biometrics [1], artificial retina [2], imaging sensors [3] and non-flat display [4]. Various approaches, therefore, have been proposed to realize functional devices on non-planar or hemispherical surfaces: transfer-based fabrications [3,5,6], self-assembly [4,8,9], interconnection of device tiles [10], and contact patterning methods [11,12]. Although all the proposed methods have demonstrated feasibility, they are not desirable to realize highly integrated and complex device structures and circuits with an acceptable fabrication yield. These strategies are limited by strain due to deformation [5–7], lack of scaling capability [3,4,8–10] and poor level-to-level alignment accuracy [11,12]. Also normal contact photolithography cannot be used for non-planar surfaces due to the substrate curvature. To circumvent these limitations, we used a combination of the proven maskless laser-write lithography (LWL) [13,14] initially developed for flat surfaces and hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) technology developed for flat-panel display to realize a-Si:H TFTs on a concave substrate. This direct LWL fabrication method is free of stress or deformation induced by transfer-based approach. High-resolution interferometer monitoring (<10 nm) and precisely controlled tilting-stage in the LWL system can provide a high level-to-level alignment accuracy [14]. In this work, we describe the fabrication of the a-Si:H TFTs with various channel widths and a channel length of 10 μm on a concave surface. The electrical characteristics and the impacts of the curvature on both TFT processing and electrical performance are described.

2. Experimental details

Fig. 1a illustrates a customized concave glass substrate used in this work; level-to-level alignment marks were placed on a flat area as indicated by gray crosses. The radius-of-curvature (ROC) is 3 cm, the field of view (FOV) is 33.5°, and the total diameter including flat area is 3 cm. This substrate will be replaced by more spherical one in near future work; the ROC is 1 cm and the FOV is 120°. Fig. 1b and c shows photographs of the fabricated devices. Prior to each LWL exposure step, the photoresist (AZ1505) was spin-coated to form a uniform coating over a curved surface; the ratio of substrate-radius (0.865 cm) to radius-of-curvature (3 cm) is below 0.816, which guarantees the spin-coated film is nearly homogeneous over the curved surface [15]. To evaluate the thickness difference of spin-coated photoresist between curved and flat areas, we partly removed the resist and measured the uniformity across the sample using a mechanical profiler. The thickness of the photoresist on a flat area (594 nm ± 20) was slightly thicker than that of a curved surface (575 nm ± 20) at 4000 rpm. This difference does not have any impact on LWL exposure conditions. However, larger film-inhomogeneity was observed over the transi-

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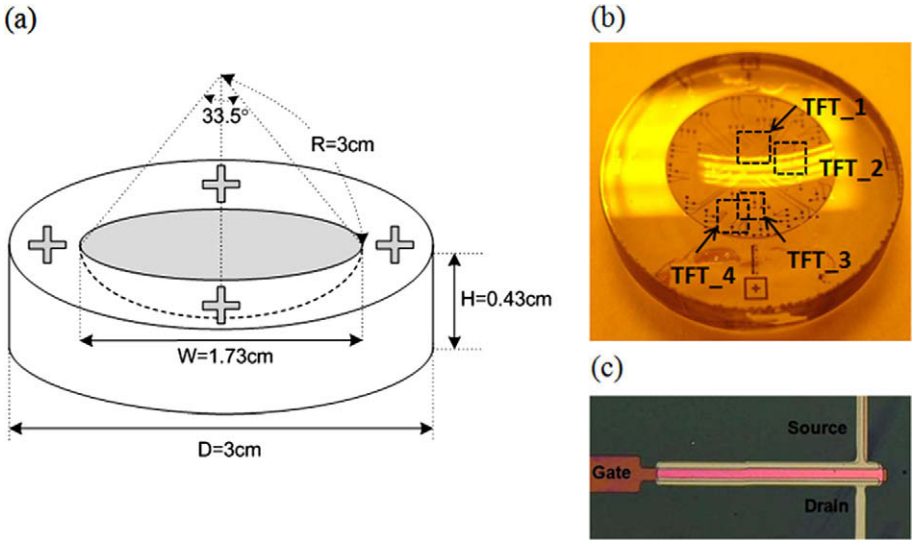

Fig. 1. (a) Illustration of the customized concave glass substrate. Crosses represent alignment marks on the flat area. (b) Photograph of the fabricated substrate. Dashed squares show the measured a-Si:H TFTs. (c) Optical microscope image of the fabricated a-Si:H TFT (W/L = 300/10) from the edge of curved surface.

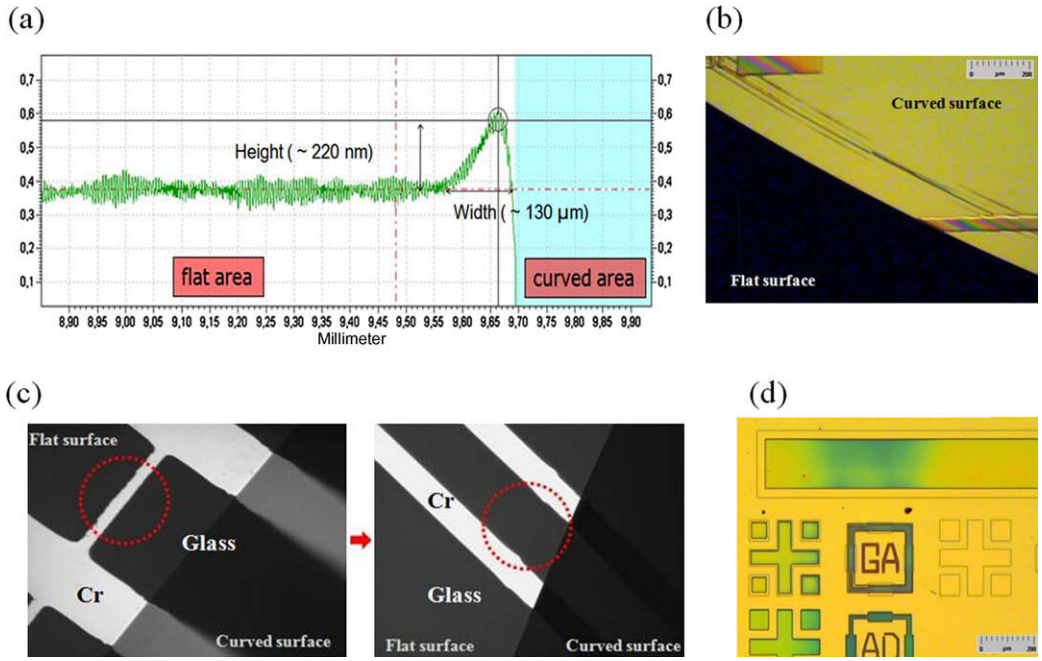

Fig. 2. (a) Thickness profile of the spin-coated photoresist over the transition area. Measured height and width of the edge-bead shown. (b) Distortion and additional connection of patterns due to edge-bead formation over the transition area between a curved and flat area. (c) Additional connection (red circle area) formed by edge bead of the photoresist was removed by the local double exposure. (d) Optical microscope image of the alignment marks after Gate electrode to Active island layer exposure. Photoresist was not removed to capture clear images. (For interpretation of the references in colour in this figure legend, the reader is referred to the web version of this article.)

tion area between curved and flat areas, and it was found to be due to edge-bead formation. The measured width and height of the formed edge-bead by mechanical profiler were in the range of 100–250 μm and 200–500 nm, respectively (Fig. 2a). These edge beads can cause additional connections, distortions of the structure size or breakup of the patterns lying over the transition area (Fig. 2b). This is due to remaining non-exposed photoresist after development process that will affect the subsequent etching process step. To correct this effect, we used the local double LWL exposure method, consisting of double exposure of the edge-bead formed areas with different light-doses. Such double exposure will allow full removal of the exposed areas during the development process in MIF 726 developer for 35 s. Hard-baking was performed in an oven at 110 °C for 10 min after each photolithography development process step. Fig. 2c shows the results before and after the local double exposure treatment. It was also found that the substrate dimension must be very well defined (±0.1 mm) to provide the reference dimension of the curved areas to be accurately local double exposed.

Following photoresist spin-coating and soft-baking in an oven at 90 °C for 5 min, LWL was used to expose all device layers before each processing step. In our experiment, a concentric-circle exposure-strategy similar to what Xie et al. demonstrated [13] was used instead of a conventional exposure method [14] which would

decompose the electronic design data into square subfields. Our strategy exposed all layers without rotating the substrate. This alternate is used because 33.5° FOV of our substrate exceeds the maximum mechanical tilt angle (20°) of the substrate table in the present LWL configuration [14], e.g. the area to be exposed cannot be perpendicular to the incident light and therefore a uniform pattern of photoresist would have been difficult to achieve. To process a substrate with higher FOV, a custom design LWL tool is needed. In this work Heidelberg Instruments DWL 400 modified for curved surfaces was used [14].

Level-to-level alignment with a high accuracy is the central critical issue for fabricating fully functional imaging devices and circuits. It was performed here in the following manner: the optical and metrology system in the LWL is equipped with two camera systems. One camera with a large field of view is used to find alignment marks located on the flat area of the substrate, and another camera with a high resolution is intended for aligning these marks. Fig. 2d shows part of the alignment marks used in this experiment. The level-to-level alignment error is defined as the relative position deviation of the alignment marks within the two following layers, and we derive vertical and horizontal deviation from the measurement of the distance of the borders on four sides in the bar alignment mark. The measured error was less than 2 μm for TFT with a 10 μm channel length and up to 300 μm channel width.

To evaluate the influence of the substrate curvature on LWL exposure accuracies, we measured dimensions of channel length, width and gate electrode line width from 'TFT_1' and 'TFT_4' in Fig. 1B. The discrepancies of dimensions between fabricated structures and an electronic design were 4.16% for 'TFT_1' and 4.88% for 'TFT_4'. No significant dependency of patterned-structures accuracy on substrate curvature was observed by virtue of the optical auto-focus system, the high resolution interferometer monitoring and precise control of the substrate table of the LWL system [14].

Uniformity evaluation of thin-film deposited by plasma-enhanced chemical vapor deposition (PECVD) and etched by reactive-ion etching (RIE) was conducted by acquiring and analyzing scanning electronic microscope (SEM) images. As illustrated in Fig 3a, after cleaving a concave substrate through the center, we took pictures of the cross section from the vertex to the edge of the curved surface with 1 mm distance between images. Fig. 3b shows an image taken from the middle of a concave surface. We then collected nine data points of thickness distribution for each layer. The thickness variations of each layer are as follows: chromium (Cr) of the gate electrode (203 nm ± 8), the tri-layer deposition of hydrogenated amorphous silicon nitride (a-SiN_X:H)/a-Si:H/p-doped a-Si:H (n+ a-Si:H) (634 nm ± 70), and the etched thickness of the active channel layer by RIE (118 nm ± 14). Although the sputtered Cr layer showed a low deviation due to a benefit of physical vapor deposition, thin-film deposition and etching by PECVD and RIE method, respectively, showed relatively higher deviation that can be due to non-uniform flow of gas mixtures over flat and curved surfaces.

First, Cr of 200 nm was deposited by a sputtering method and then the Cr gate electrode was patterned by wet-etching using CR-14 (CH_3COOH:$Ce(NH_4)_2(NO_3)_6$:H_2O in 9:22:69) etchant (layer #1). Next, PECVD was used to deposit a tri-layer of gate silicon nitride (a-SiN_X:H, 400 nm) forming a gate insulator together with amorphous silicon (a-Si:H, 170 nm) and phosphorous-doped (n+) a-Si:H (70 nm) forming an active channel layer. The active island was defined by RIE dry-etching of a-Si:H and n+ a-Si:H using a gas mixture of SF_6 and O_2 (layer #2). Following a deposition of a source/drain (S/D) metal Cr layer (130 nm) by a sputtering method, wet-etching using CR-14 etchant was done to form S/D contacts (layer #3). Then to remove the n+ a-Si:H layer from the channel region, back-channel etching is performed by RIE dry-etching with a gas mixture of SF_6 and O_2 using the S/D metal and a photoresist as a mask. We subsequently defined contact via to the gate electrode using buffered hydrofluoric acid (BHF) (layer #4). As a final step, thermal annealing was performed at 250 °C for an hour to improve electrical properties of each film layer [16]. We note that for each processing step photoresist (AZ1505) was first spin-coated over deposited layers, and then exposed using LWL to realize level-to-level alignments. Finally, the photoresist was stripped using PRS-2000. Electrical measurements were conducted and analyzed using probe station in combination with HP4156 at room temperature in dark condition.

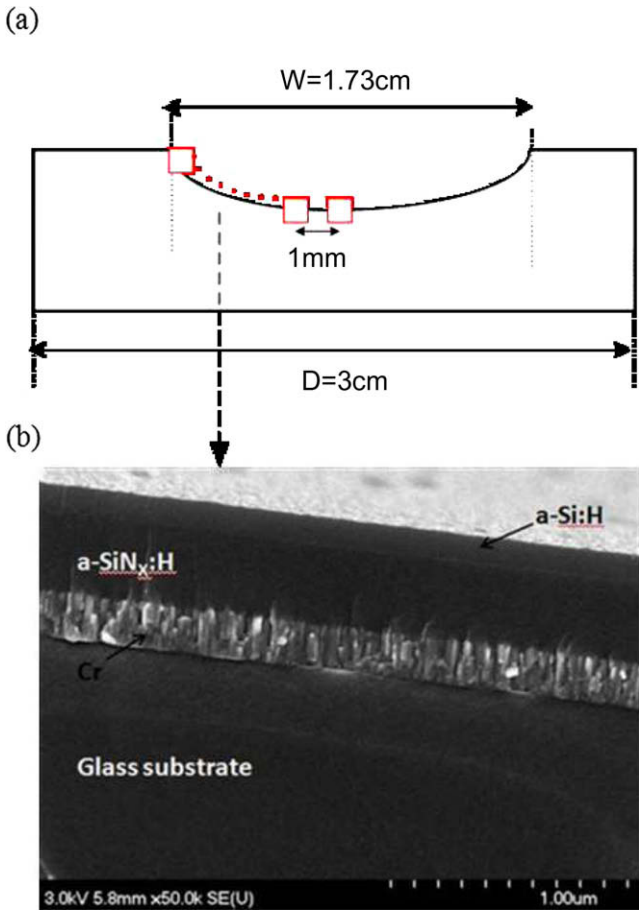

Fig. 3. (a) Illustration of the method used to get cross-sectional images of the curved surface. (b) Scanning Electronic Microscope image captured in the middle of curved area.

3. Experimental results and discussion

As indicated in Fig. 1B, a-Si:H TFTs at different locations were characterized to evaluate the impacts of the substrate curvature on the device electrical properties. Fig. 1C shows the fabricated a-Si:H TFT (W/L = 300/10, 'TFT_2'). We first measured the output characteristics of the TFT for various gate voltages, V_{GS} = 0, 5, 10 and 15 V (Fig. 4a). For the low V_{DS} bias (0–2 V), Fig. 4b shows the output characteristics and output conductance defined as the derivative of the drain-to-source current (I_{DS}) with respect to drain voltage (V_{DS}). We swept V_{DS} from 0 to 15 V and I_{DS} exhibits typical output characteristics. The transfer characteristics for various drain voltages (V_{DS} = 0.1, 1, 10 V and V_{GS}) were measured, and the data at V_{DS} of 0.1 V and V_{GS} correspond to a linear and saturation operating regime, respectively. We used the 10–90% range data of the maximum I_{DS} for the extraction of threshold voltage (V_{th}) and field-effect mobility (μ_{FE}) in Fig. 4c. OFF-current (I_{OFF}) was extracted at

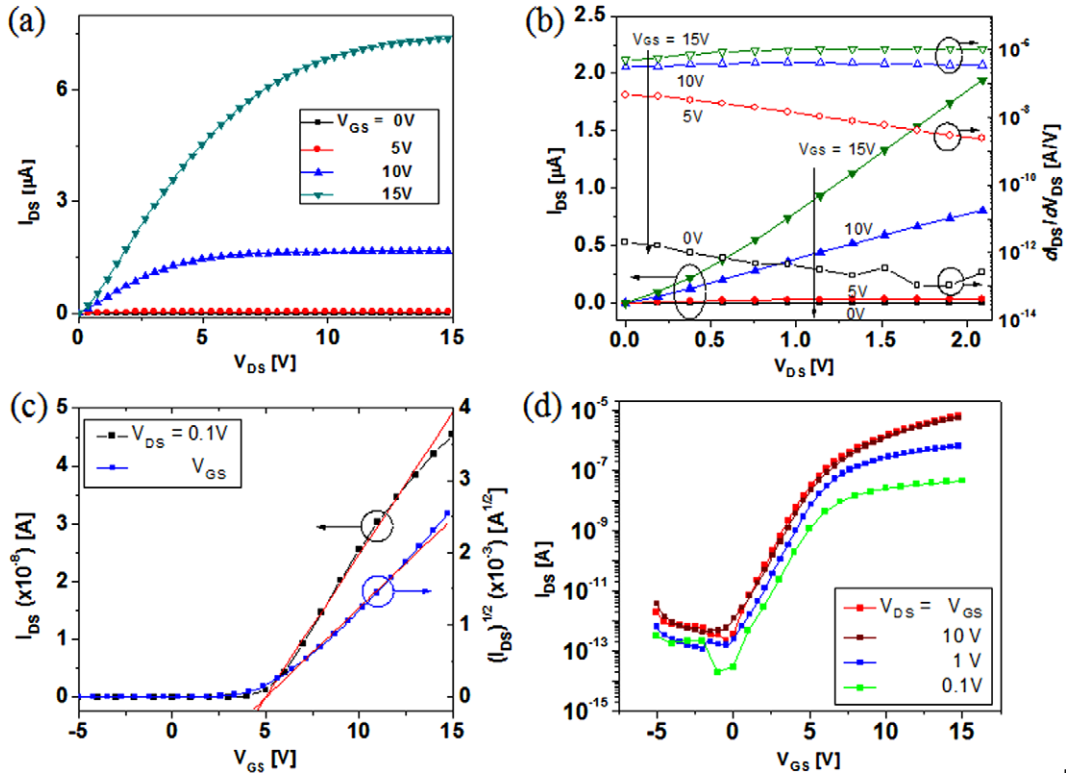

Fig. 4. Electrical properties of the fabricated a-Si:H TFT (W/L = 300/10). (a) Output characteristics. (b) Output characteristics and output conductance in low V_{DS} bias region (0–2 V). (d) Transfer characteristics with fitting lines used for extractions of threshold voltage and mobility. (d) Transfer characteristics in a log scale.

Table 1
Variation of the extracted parameters of the fabricated a-Si:H TFTs.

Parameters	V_{DS} = 0.1 V	V_{DS} = V_{GS}
I_{OFF} [A] at V_{GS} = −5 V	$3.2 \times 10^{-13} \pm 1 \times 10^{-13}$	$5.5 \times 10^{-12} \pm 4.5 \times 10^{-12}$
V_{th} [V]	6.9 ± 1.8	5.7 ± 2
S [V/dec]	1.21 ± 0.14	1.04 ± 0.2
μ_{FE} [cm^2/V s]	0.1 ± 0.02	0.21 ± 0.07

V_{GS} = −5 V, and subthreshold swing (SS) was derived from the inverse of maximum slope in subthreshold region (Fig. 4d). Other a-Si:H TFTs were measured and analyzed using the same approach. The variations of extracted TFT parameters are summarized in Table 1.

For a linear (V_{DS} = 0.1 V) and saturation (V_{DS} = V_{GS}) regimes, the variations in V_{th} were ±26% and ±35%, respectively; the variations in μ_{FE} were ±20% and ±33%, respectively; the variations in I_{OFF} were ±31% and ±80%, respectively; the variations in SS were ±12% and ±19%, respectively. These variations can be associated with the variation of the a-Si:H thickness (t_{si}) over the curved surface (153 ± 39 nm) after back-channel dry-etching [17]. With an increase of the t_{si} in the dry-etched a-Si:H TFT, it is observed that V_{th}, SS and μ_{FE} tend to decrease [18]. The variation of the t_{si} can be resolved by further optimizing dry-etch conditions or adopting isotropic wet-etching methods which are independent from the surface curvature.

4. Conclusions

In summary, the a-Si:H TFTs with a 10 μm channel length on the concave surface were fabricated using the maskless laser write lithography; a high level-to-level alignment accuracy (±2 μm or less) was also demonstrated for fabricated devices. The electrical performances of the fabricated a-Si:H TFTs were characterized over the curved surface. Due to the thickness variation of the dry-etched a-Si:H layer over the curved surface, changes in OFF-current, field-effect mobility, subthreshold swing and threshold voltage were observed. These variations are acceptable for development of the imager on non-planar surfaces. The TFT maskless fabrication method described in this paper is suitable for fabrication of a high density TFT pixel arrays and circuits to be fabricated on a hemispherical surface for image sensors.

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